TB-FMCL-MIPI with camera OV13850CLGA-BSI_AA Application Note

Rev.1.00

Revision History

Version	Date	Description	Publisher
Rev.1.00	3/03/2016	Initial release	MT

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Note: All documents relating to TB-FMCL-MIPI board can be downloaded from the TED Support Web at address https://www.teldevice.co.jp/spweb/c0201s

1. Overview and Clarifications

This document talks about the TB-FMCL-MIPI (variant CSI/DSI) board connected through TB-OV13850-ADAPTER board to camera OV13850CLGA-BSI_AA.

For the TB-FMCL-MIPI board:
The MIPI CSI port goes through connector J5.
The MIPI DSI port goes through connector J16.
The MIPI connectors are LSHM-120-01-F-DH-A-N-K-TR

For the TB-OV13850-ADAPTER board:
The connector matting with the TB-FMCL-MIPI board is J10, Samtec PN:
LSHM-120-03.0-F-DV-A-S-K-TR.

Below is the pin numbering convention for the connectors.

On the TB-FMCL-MIPI board:

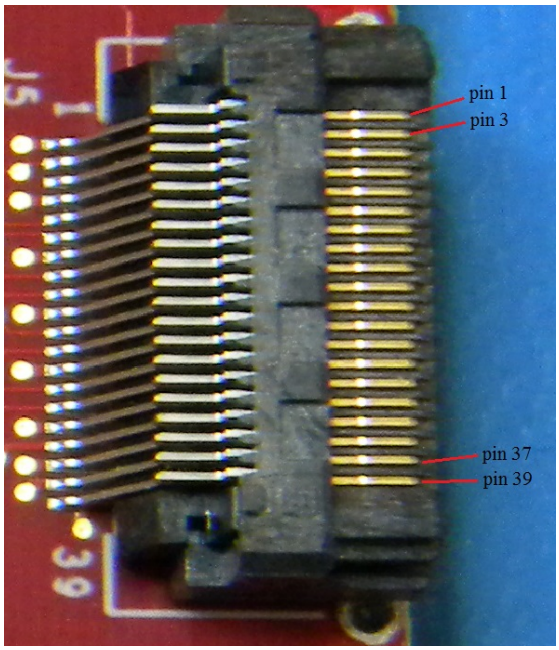


Figure 1-1 LSHM-120-01-F-DH-A-N-K-TR pin numbering

On the camera adapter board:

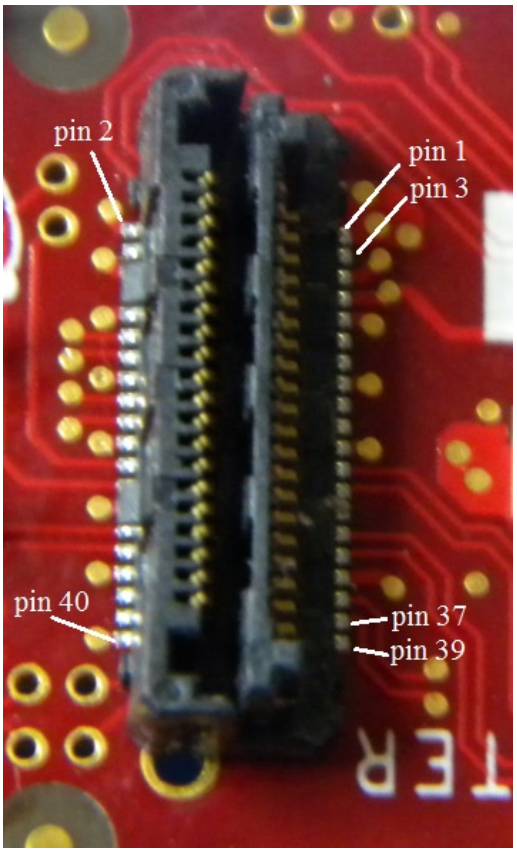


Figure 1-2 LSHM-120-03.0-F-DV-A-S-K-TR pin numbering

As the pin numbering from the connector manufacturer can be difficult to follow, the table below lists the pins and associated nets name mapping.

Table 1-1 Pin numbers and net name mapping

J10 -LSHM_DV	Net Name	J5 -LSHM_DH	Net Name
1	12V0	40	12V0
3	3V3	38	3V3
5	GND	36	GND
7	VUSER	34	VUSER
9	GND	32	GND
11	MIPI_SLVS_IN0_BTA_P	30	MIPI_SLVS_IN0_BTA_P
13	MIPI_SLVS_IN0_BTA_N	28	MIPI_SLVS_IN0_BTA_N
15	GND	26	GND
17	MIPI_SLVS_IN1_P	24	MIPI_SLVS_IN1_P
19	MIPI_SLVS_IN1_N	22	MIPI_SLVS_IN1_N
21	GND	20	GND
23	MIPI_SLVS_IN2_P	18	MIPI_SLVS_IN2_P
25	MIPI_SLVS_IN2_N	16	MIPI_SLVS_IN2_N
27	GND	14	GND
29	MIPI_SLVS_IN3_P	12	MIPI_SLVS_IN3_P

J10 -LSHM_DV	Net Name	J5 -LSHM_DH	Net Name
31	MIPI_SLVS_IN3_N	10	MIPI_SLVS_IN3_N
33	GND	8	GND
35	MIPI_SLVS_IN4_P	6	MIPI_SLVS_IN4_P
37	MIPI_SLVS_IN4_N	4	MIPI_SLVS_IN4_N
39	GND	2	GND
2	GND	39	GND
4	3V3	37	3V3
6	GND	35	GND
8	VUSER	33	VUSER
10	GND	31	GND
12	CLK_I2C_SCL_MIPI_CSI_OD	29	CLK_I2C_SCL_MIPI_CSI_OD
14	I2C_SDA_MIPI_CSI_OD	27	I2C_SDA_MIPI_CSI_OD
16	GND	25	GND
18	FSIN	23	MIPI_AUXIO_1
20	PWDN_OR_XSHUT	21	MIPI_AUXIO_2
22	GND	19	GND
24	STROBE	17	MIPI_AUXIO_3
26	FREX	15	MIPI_AUXIO_4
28	GND	13	GND
30	LOOP_P	11	LOOP_P
32	LOOP_N	9	LOOP_N
34	GND	7	GND
36	NC	5	NC
38	NC	3	NC
40	GND	1	GND

1.1. Jumper settings for TB-FMCL-MIPI board

As there are many configuration jumpers on the MIPI FMC, to avoid damage, it is imperative that they be set correctly for the application.

Note: The camera OV13850CLGA-BSI_AA requires a 1.8V signal interface level, this will be the basis of the jumper configuration approach.

To understand how to place the jumpers on J9, J6, J12, J17 and J19 see block diagram below.

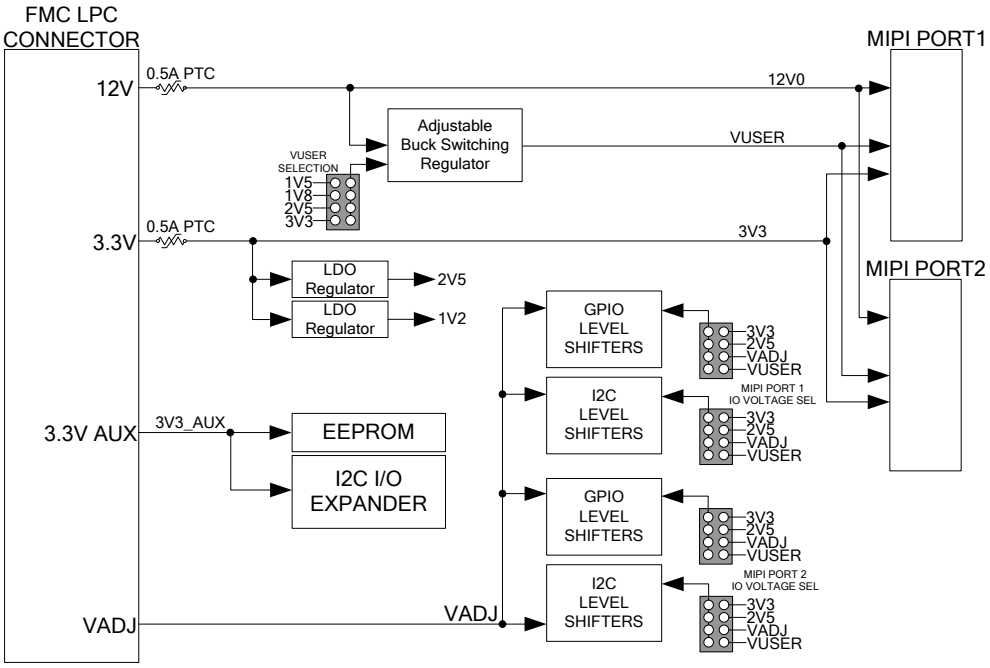
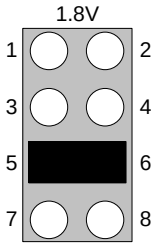
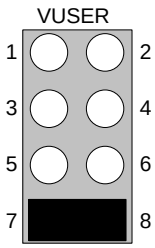
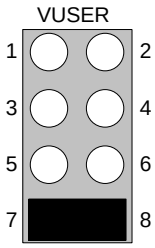
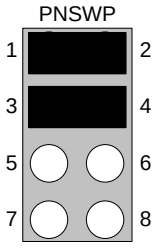


Figure 1-3 TB-FMCL-MIPI Power Structure

For use of the camera OV13850CLGA-BSI_AA adapter, the following jumper settings are recommended:

Note: Positioning more than one shunt, or positioning a shunt in a position not described above could result in permanent damage to the board.

Table 1-2: Jumper settings to interface camera OV13850CLGA-BSI_AA

Jumper	Function	Setting
J9	Sets the VUSER voltage VUSER is set for 1.8V	
J6	PortA I2C interface voltage setting =VUSER for this adapter	
J12	PortA GPIO interface voltage setting =VUSER for this adapter	
J17	PortB I2C interface voltage setting	Not applicable. This jumper does not impact the operation of PortA (CSI Port). The setting is impacted by only the PortB requirements.
J19	PortB GPIO interface voltage setting	Not applicable. This jumper does not impact the operation of PortA (CSI Port). The setting is impacted by only the PortB requirements.
J3	Sets the PNSWP input level on the Meticom PHY. Note that pins 1 and 2 impact the Meticom device on PortA (the CSI port), and is to be configured as shown. Pins 3 and 4 only impact the the Meticom device on PortB (the DSI port), so default position is shown.	

When properly configured for PortA to interface to the camera OV13850CLGA-BSI_AA adapter, the board will look as follows:

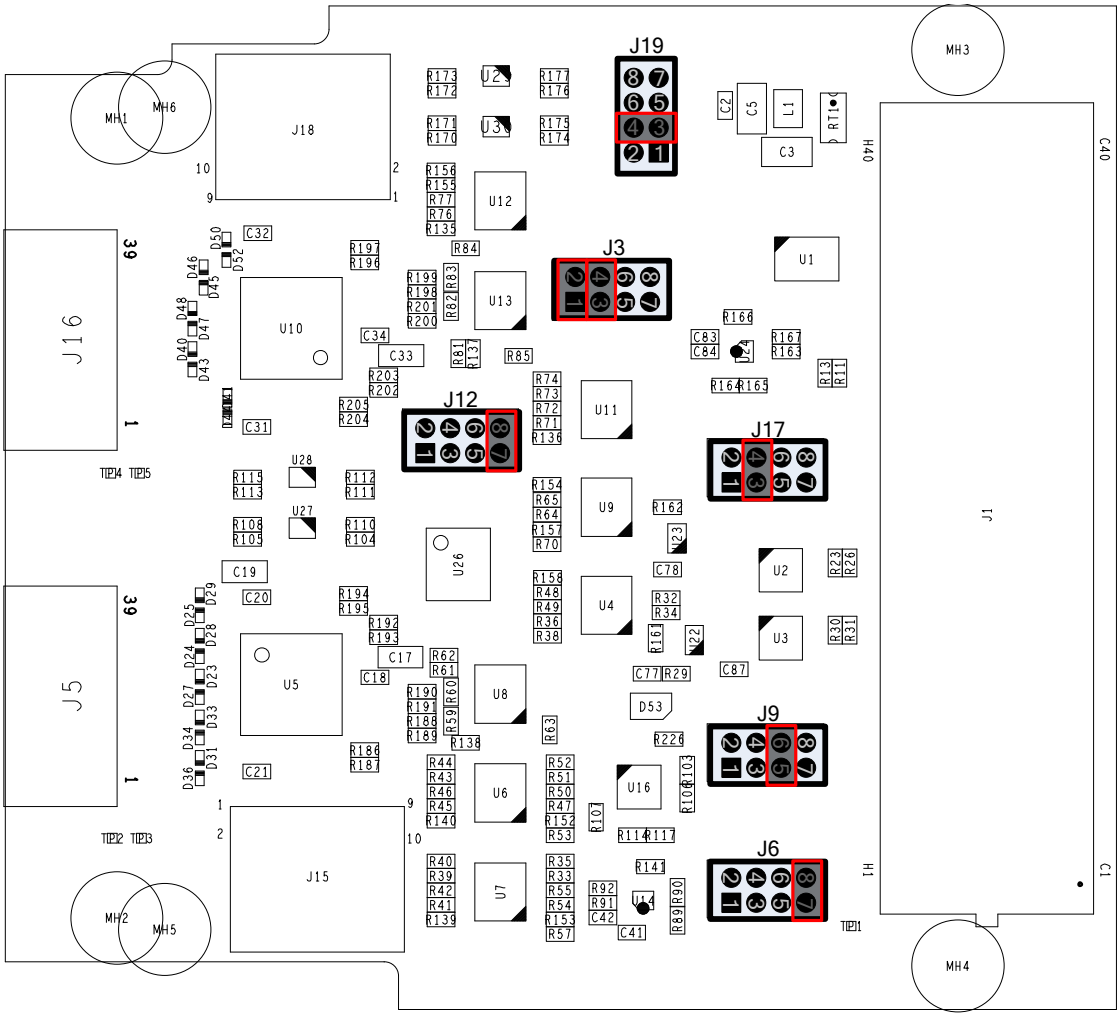
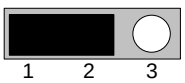


Figure 1-4 Jumper Positions and Header Orientation

1.2. Jumper settings for TB-OV13850-ADAPTER board

Table 1-3: Jumper settings for adapter board -J12

Jumper	Function	Setting
J12	Jumper across pins 1 and 2 (PWDN_OR_XSHUT=PWDN)	

1.3. Interfacing Photo

The next photo shows a camera connected to the TB-FMCL-MIPI board:

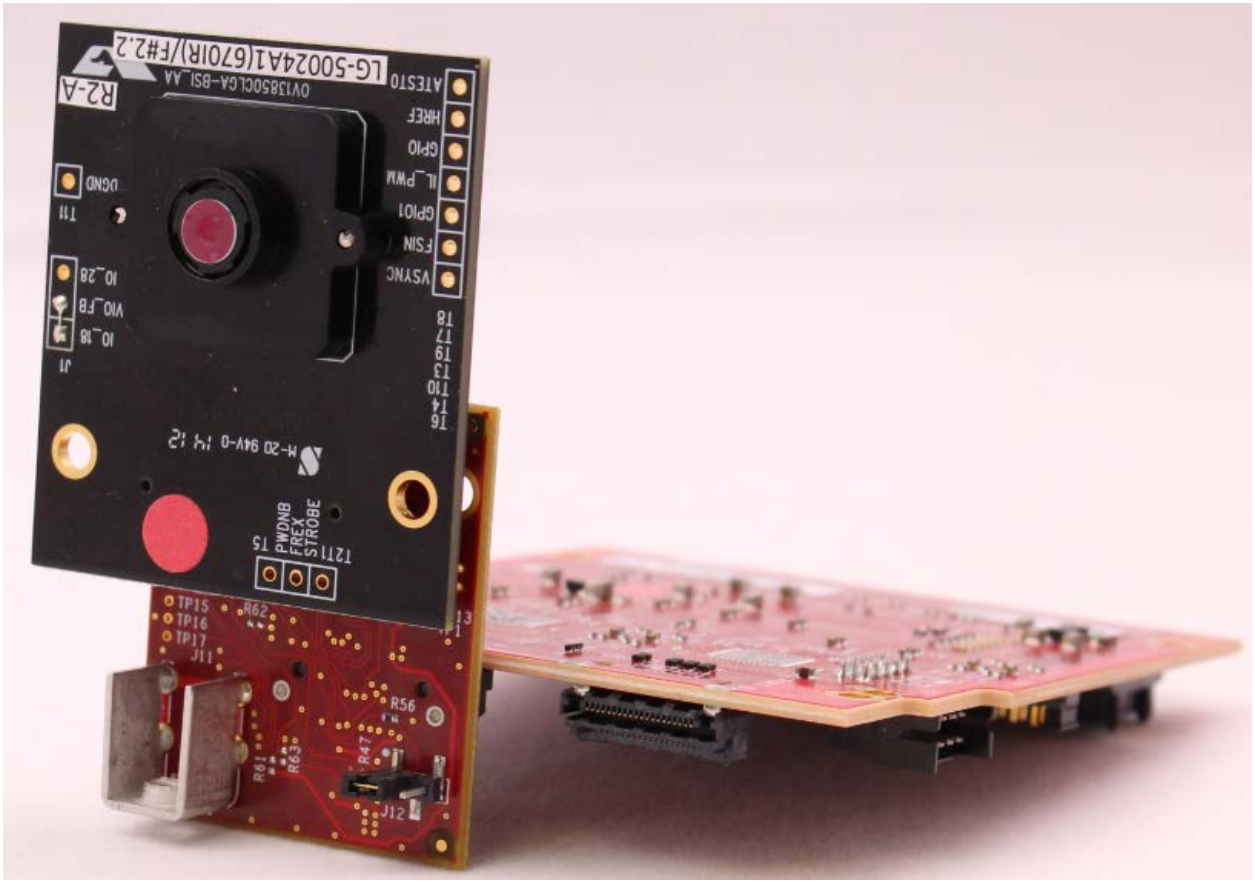


Figure 1-5 Camera OV13850CLGA-BSI_AA Assembly

2. CSI Reference Design Setup Guide

2.1. Requirements

2.1.1. Hardware Requirements

CSI to HDMI reference design requires the following hardware:

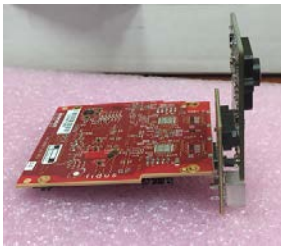
- Xilinx Virtex-7 VC707, revision 1.0 board and power supply
- TB-FMCL-MIPI board + TB-OV13850-ADAPTER board
- OmniVision OV13850 board
- USB cable Type-A to micro-B
- HDMI cable
- Monitor with HDMI support

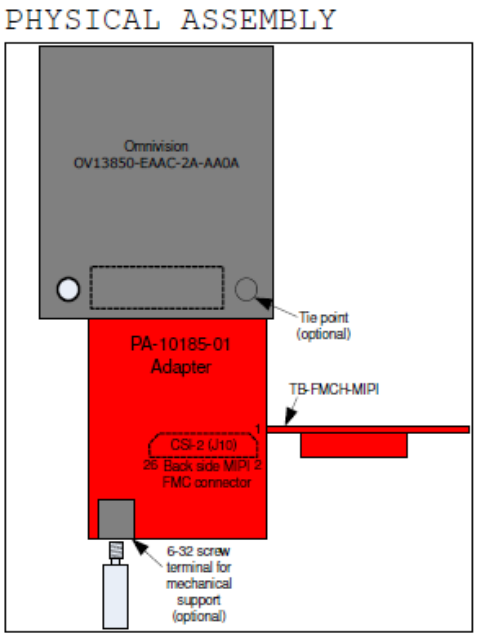
2.1.2. Software Requirements

- Vivado Lab Edition

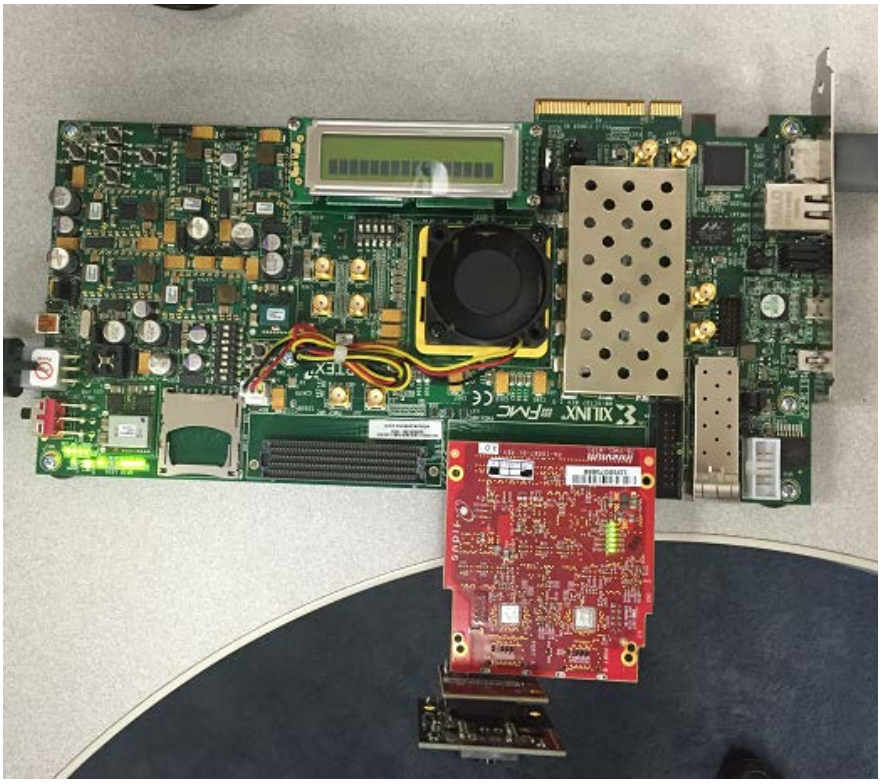
2.2. Hardware Setup

1. Connect the OmniVision OV13850 module to the J9 QSE connector on TB-OV13850-ADAPTER board.
2. Connect the CSI Adapter board to the J5 LSHM connector on the TB-FMCL-MIPI board.



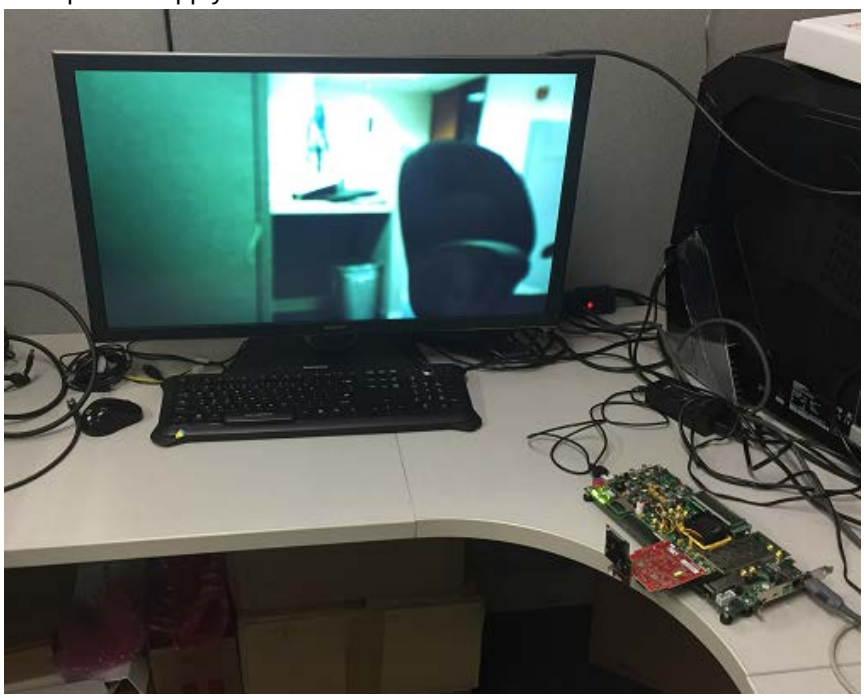


3. Connect the TB-FMCL-MIPI module to the HPC FMC1 connector on the VC707 board.



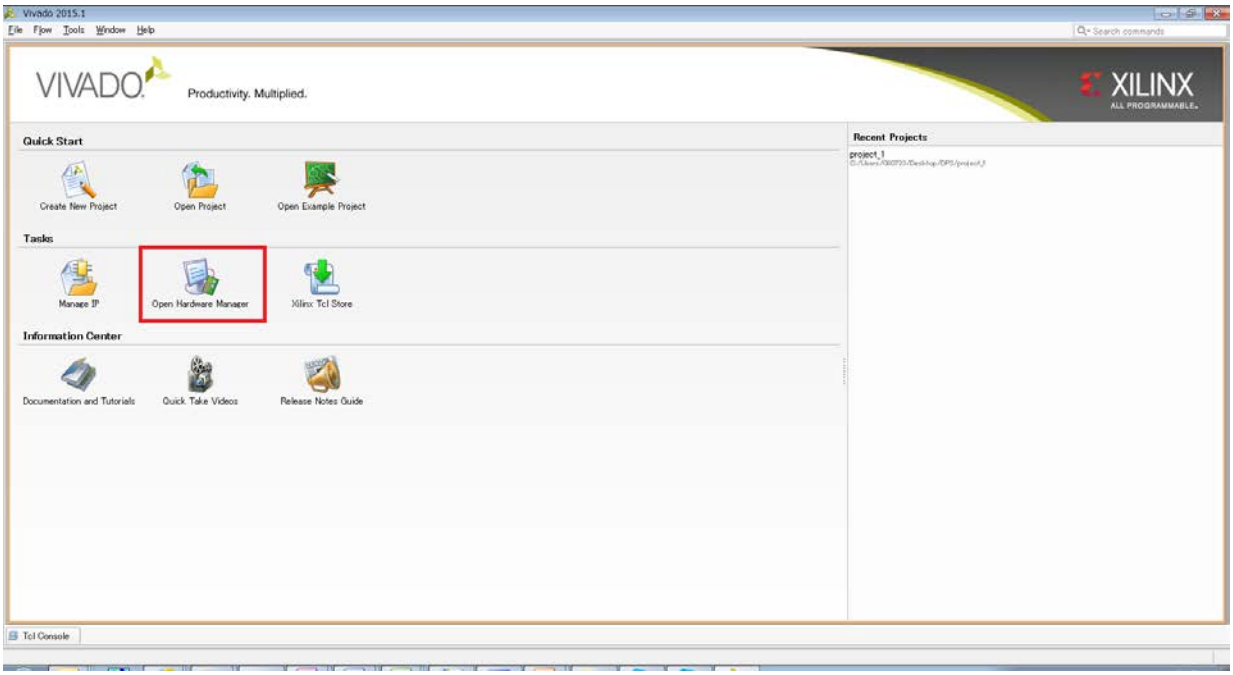
4. Connect a USB Type A to Micro B cable from the host PC to the VC707 board for programming the bit file.
5. Connect the HDMI cable to the Monitor.

6. Connect the power supply cable and turn on the VC707 board.

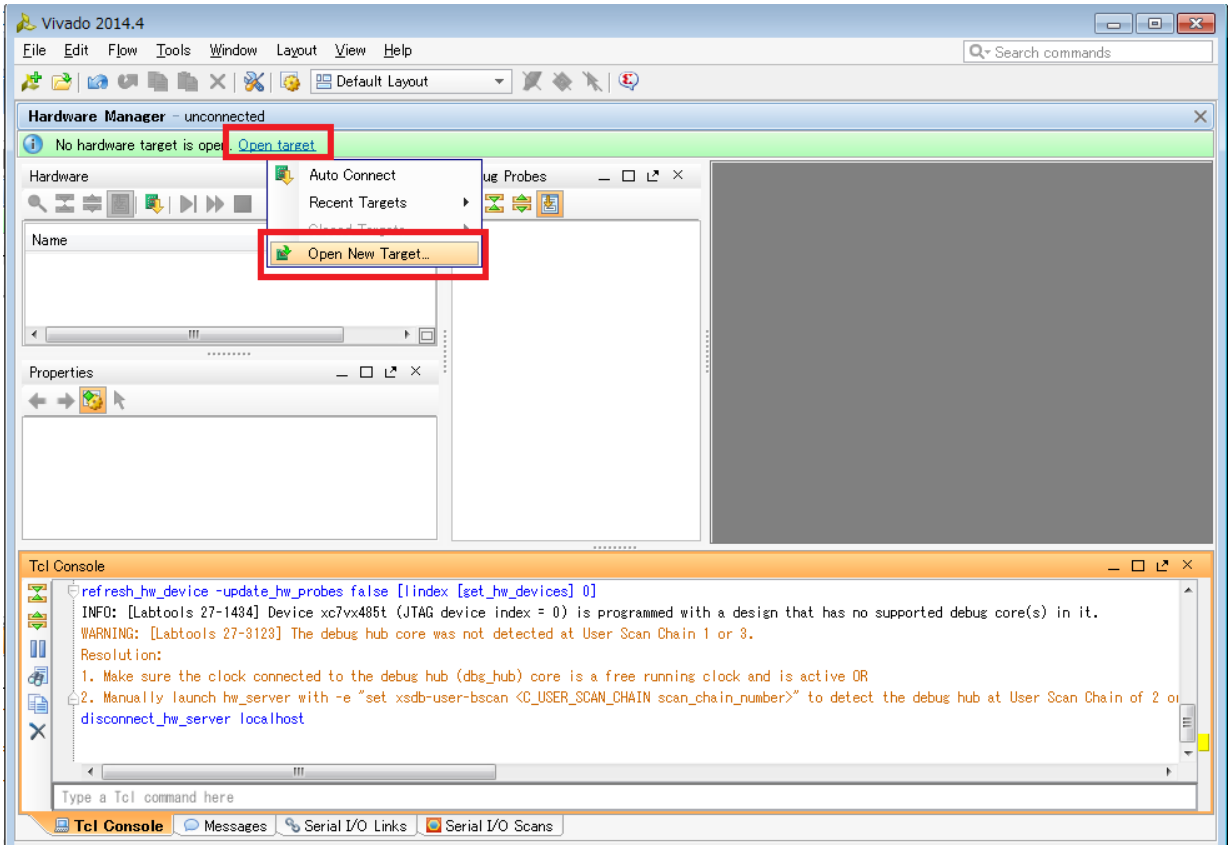


2.3. FPGA Programming

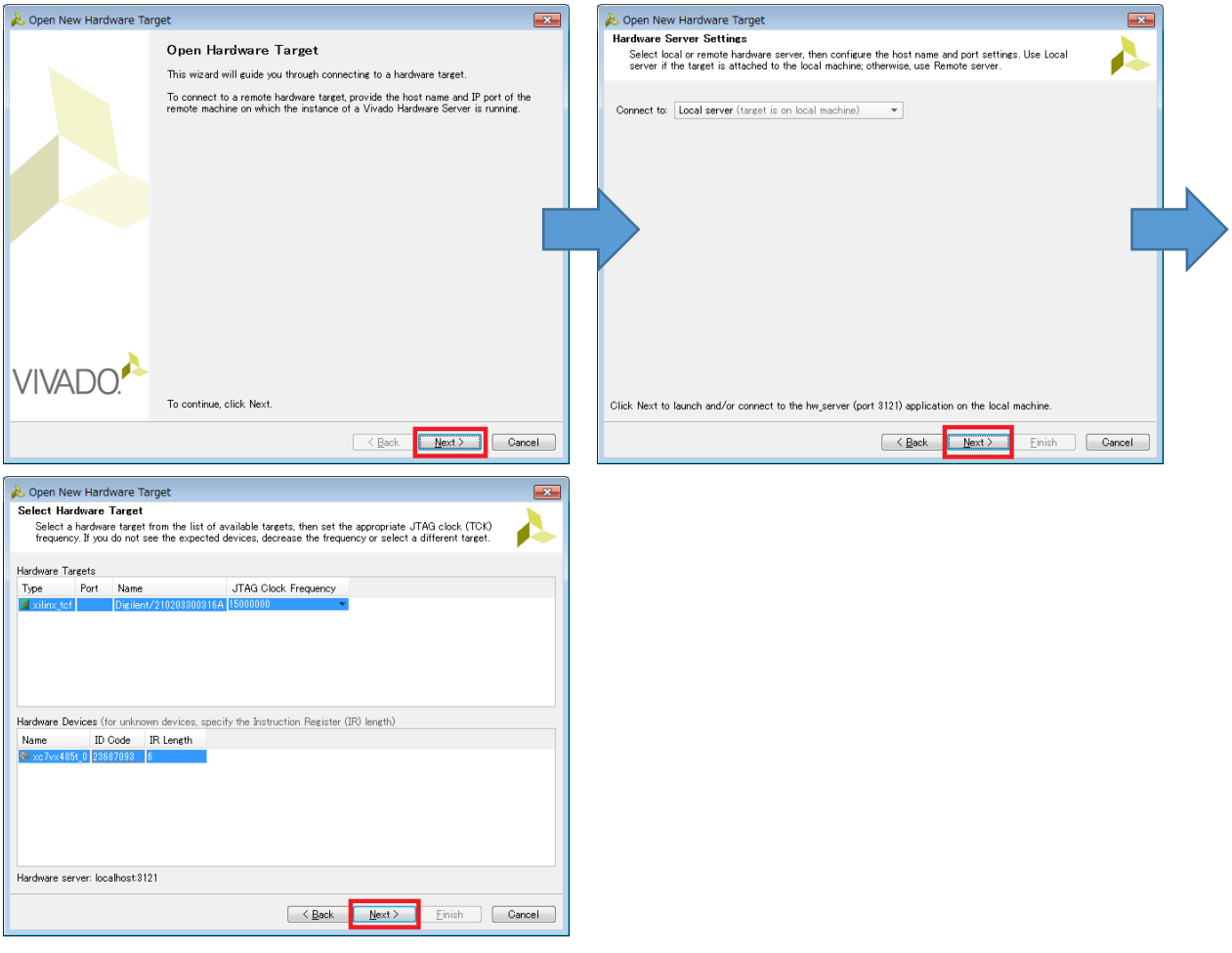
1. Open Vivado and Open Hardware Manager.



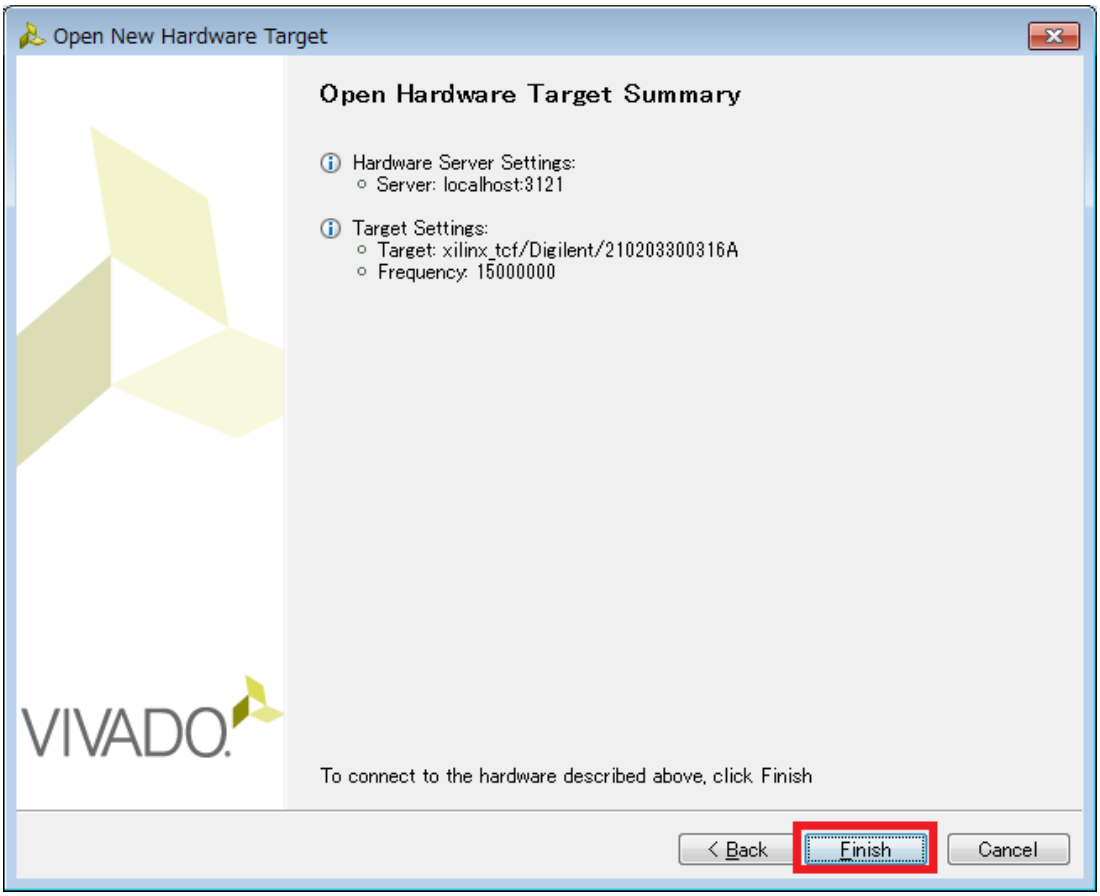
2. Open target and Open New Target.



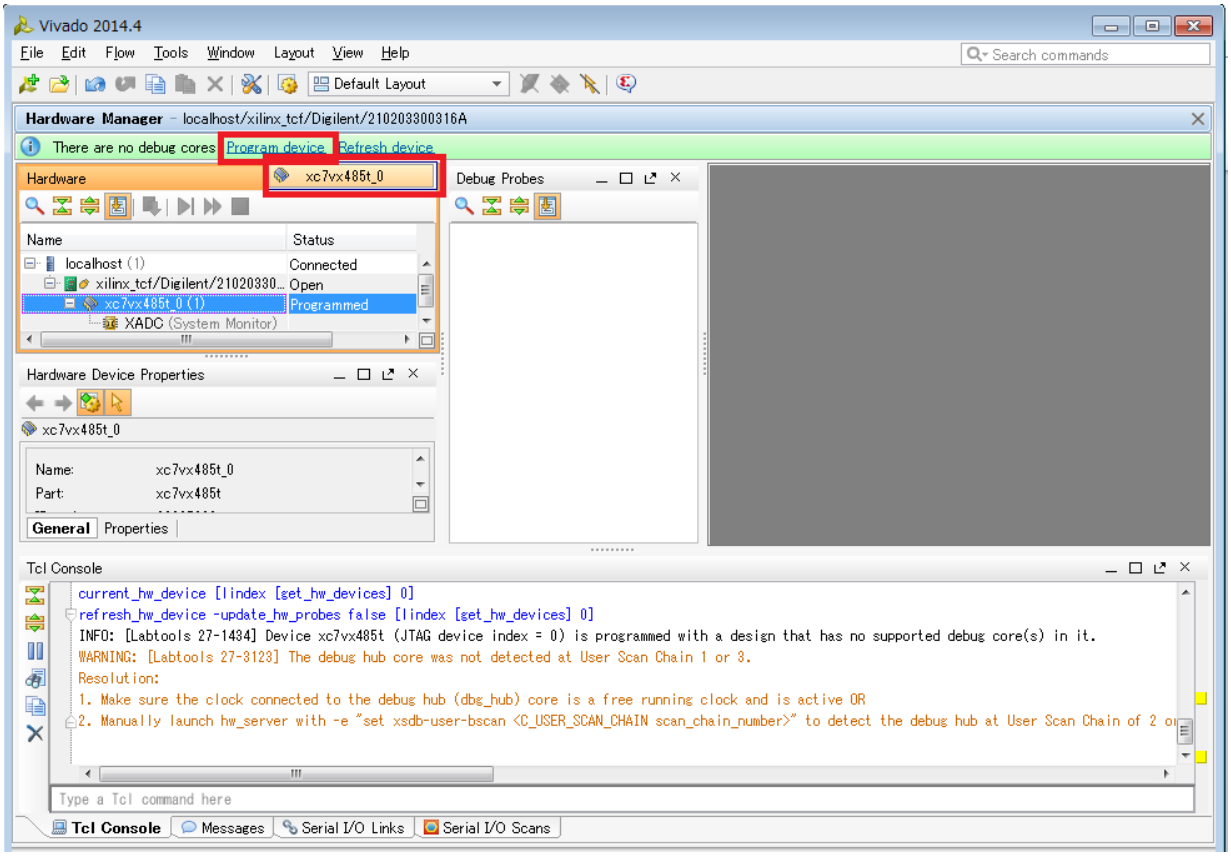
3. Click Next.



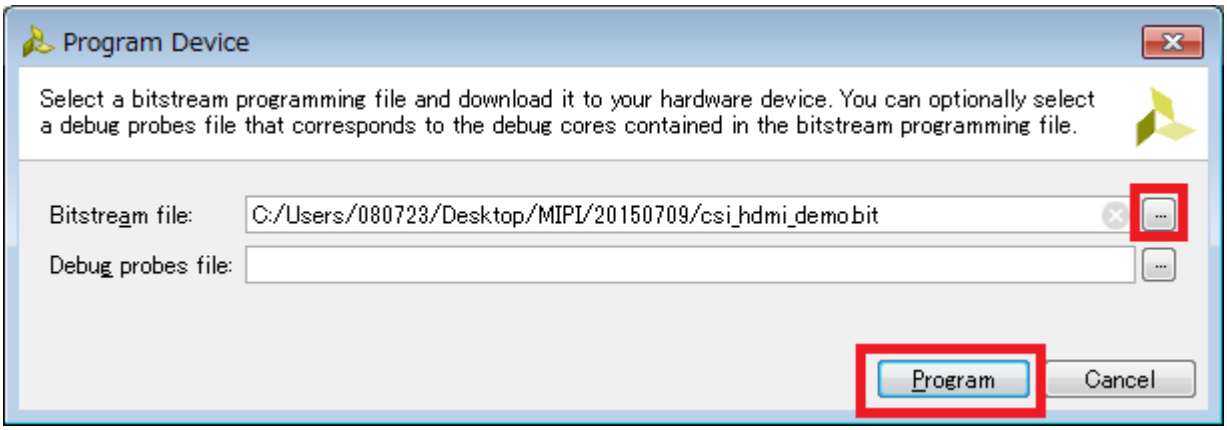
4. Click Finish.



5. Program device -> xc7vx485t_0



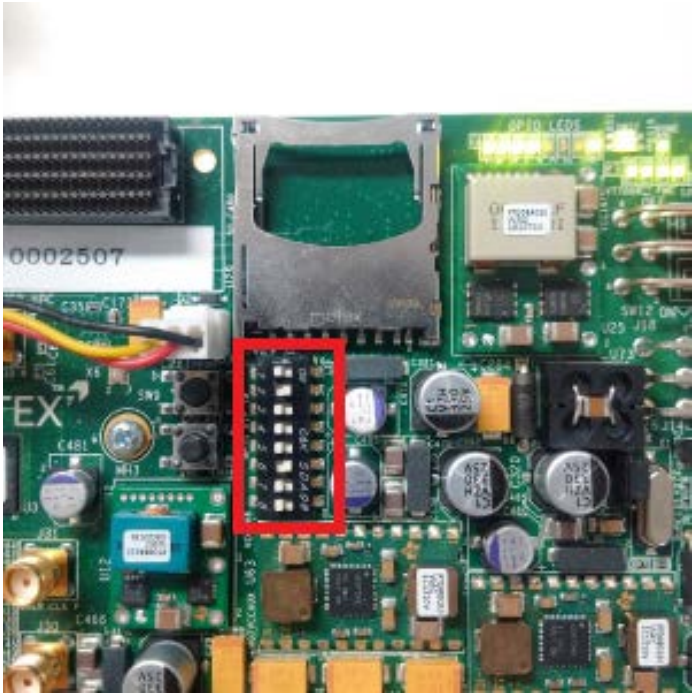
6. Select “top_csi2_dsi.bit” bitstream and program.



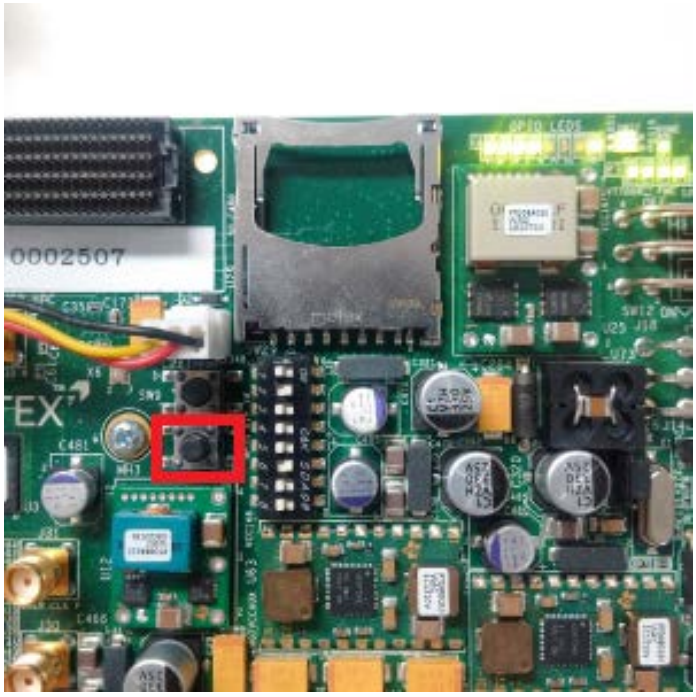
2.4. VC707 Board Settings

1. Set DIP Switch SW2.

SW2	Status
1	Off
2	On
3	Off
4	Off
5	Off
6	On
7	Off
8	Off

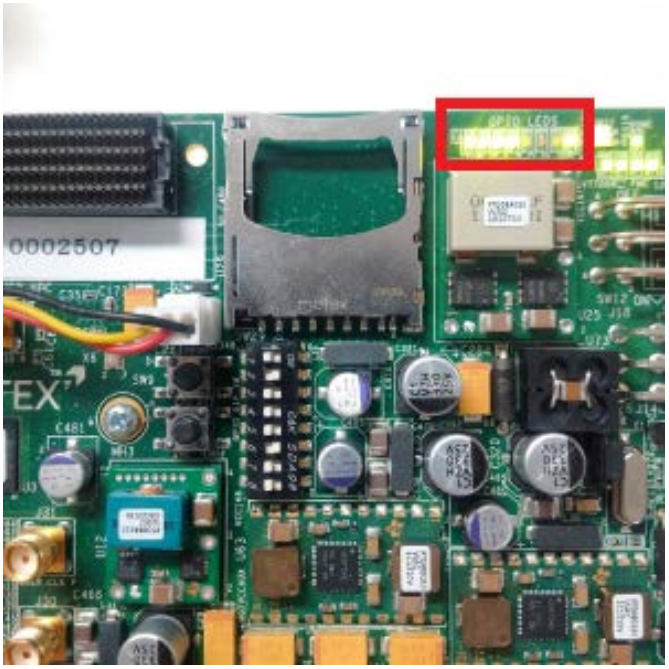


2. Push SW8.

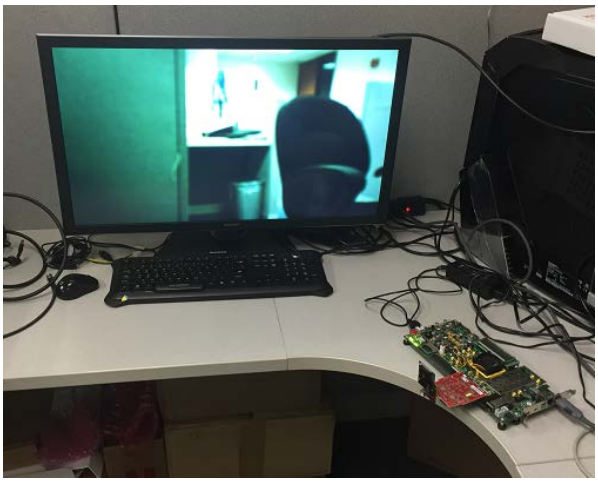


3. Check LEDs.

LED	Status
7	On
6	On
5	Fast flash
4	Fast flash
3	Off
2	Off
1	Off
0	Fast flash



2.5. Result for CSI to HDMI with Full HD (1080p 60Hz)



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